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GRT-duplex: A Novel SDR Platform for Full-Duplex WiFi

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Abstract Full-duplex wireless communication enables concurrent transmission and reception over the same radio channel. It thus achieves higher efficiency in spectrum utilization compared with its half-duplex counterpart. In recent years, researchers have built several platforms for full-duplex wireless communications. However, none of these platforms provides full support for full-duplex WiFi, arguably the most popular wireless local-area networking technology. In this paper, we present GRT-duplex, a novel full-duplex wireless platform for the WiFi family, which possesses both *flexibility* and *real-time* features. We have also prototyped a full-duplex WiFi instance on this platform, which delivered throughput up to 92.45Mbps, and the frame interaction intervals can be as small as 9.85us.

Keywords Full-duplex WiFi · Platform · Flexible · Real-time

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1 Introduction

In recent years, the radio spectrum has become overcrowded with the increasing popularity of wireless Internet access. Both user demand and scarce spectrum resource call for more efficient wireless technologies, which can achieve higher efficiency of spectrum utilization. In conventional wisdom, it is generally not feasible for radios to simultaneously receive and transmit over the same frequency channel due to the interference from its own transmission to the received signal. Therefore, the state-of-the-art commercial wireless devices only work in the half-duplex mode. However, recent studies have shown that full-duplex wireless transmission is feasible. There have been several implementations by various research groups. To this end, full-duplex wireless communication holds great promises, since it theoretically doubles the spectrum efficiency of its half-duplex counterpart.

In the WiFi context, researchers need appropriate platforms to explore full-duplex WiFi. In a nutshell, full-duplex WiFi platforms need to meet two design requirements: *flexiblility* and *real-time* processing. Specifically, flexible platforms help researchers to prototype and assess different algorithms at fast pace and with low cost, while real-time platforms ensure high throughput and low latency in processing. In recent years, researchers have built several platforms for full-duplex wireless communications [3, 5–8]. Unfortunately, none of such platforms, no matter whether it is based on software or relies on hardware, can meet both requirements.

In this paper, we propose GRT-duplex, a novel software-defined radio (SDR) platform for full-duplex WiFi that achieves both goals. GRT-duplex can meet the strict timing requirement of 802.11a/g protocols, work in the 20MHz bandwidth, and respond to a received frame in 16us (i.e.,

within SIFS, which is the fine time granularity stipulated for 802.11 a/g [2]). Moreover, GRT-duplex adopts a flexible module structure, upon which a full 802.11a/g physical (PHY) layer module library is offered. As a result, researchers can readily add, delete, or modify any module, and connect these modules at ease. This makes the platform flexible enough to enable researchers to design and refine full-duplex WiFi, while meeting the real-time requirement.

We have completed the implementation of the GRT-duplex platform, and prototyped a full-duplex WiFi instance on it. The prototype supports 20MHz bandwidth operation, and offers various modulation/demodulation schemes, including BPSK, QPSK, 16QAM, and 64QAM, for standard 802.11a/g frames in the full-duplex mode. Our system further delivers throughput up to 92.45Mbps, about 1.7 times compared with the half-duplex 802.11a/g standards, while the frame interaction intervals can be as small as 9.85us, achieves the SIFS interval requirement.

The remainder of this paper is organized as follows. Section 2 introduces the full duplex technology and the 802.11 protocol standards, and compares with the existing full-duplex WiFi platform. Section 3 describes the designs for GRT-duplex platform and full-duplex WiFi. Section 4 presents the Implementation for GRT-duplex platform, and Section 5 evaluates our platform. Finally, Section 6 discusses related issues and Section 7 concludes the paper.

2 Background

2.1 Full-duplex technology

A major challenge for full-duplex wireless systems is self-interference cancellation. To enable full-duplex communications, the device has to cancel the self-interference that originates from its own transmissions to the received signal. As a device acquires the full knowledge from its own transmitter to the receiver, the receiver can completely cancel the self-interference in theory [5, 7].

Self-cancellation can be broadly divided into three categories: antenna cancellation, analog cancellation and digital cancellation, as showed in Fig. 1. With antenna cancellation, we fully utilize the directionality and polarizability of the antenna, and the interference patterns over space caused by two or more transmissions deliver the same signal. In analog cancellation, with analog cancellation circuit, target signal and interference signal can be distinguished. So, with carefully designed antenna and radio-frequency (RF) circuit, self-interference can be significantly reduced. The residual interference will be eliminated by digital process. In this paper, we focus on the digital cancellation process.

Since the receiver captures a superimposed signal, to obtain the target signal, the receiver should first get the

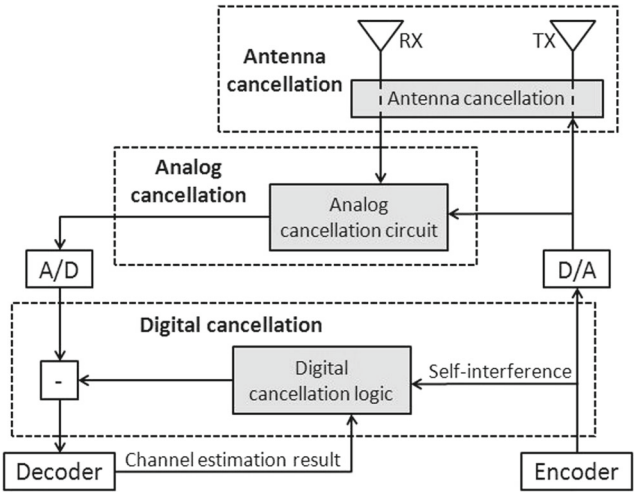

Fig. 1 Block diagram of full-duplex system

whole knowledge of both the target and the interference channel state. Typically, digital cancellation requires two steps. First, before two devices sending frame simultaneously, the preamble signals are to be sent separately. Target channel and Interference channel can be denoted by $H_t(k)$ and $H_i(k)$ separately, where k indicates the index of subcarrier in OFDM signals. We use $P_t(k)$ and $P_i(k)$ to represent the preamble signals transmit from target transmitter and itself separately. Received preambles are denoted by $Y_t(k)$ and $Y_i(k)$. By ignoring the impression of the noise and the frequency offset, the transmission process can be written by Eqs. 1 and 2.

$$Y_t(k) = P_t(k) \cdot H_t(k) \tag{1}$$

$$Y_i(k) = P_i(k) \cdot H_i(k) \tag{2}$$

In this first step, both the target channel and the interference channel are estimated using the following Eqs. 3 and 4.

$$H_t(k) = \frac{Y_t(k)}{P_t(k)} \tag{3}$$

$$H_i(k) = \frac{Y_i(k)}{P_i(k)} \tag{4}$$

In practice, the WiFi setting within a small time interval (say, a few milliseconds) can be approximately modeled as a slow time-varying channel. Assume that the wireless channel is constant in these two steps. The simplified received model can be expressed by Eq. 5, where $Y(k)$ is the received signal, $S(k)$ is the target signal and $I(k)$ denotes the interference signal from its own.

$$Y(k) = S(k) \cdot H_t(k) + I(k) \cdot H_i(k) \tag{5}$$

Second, using the channel information, we can obtain the target signals by subtracting self-interference from the

received signals [5, 7]. Equation 6 shows the mathematical model of the digital cancellation process.

$$S(k) = \frac{Y(k) - I(k) \cdot H_i(k)}{H_t(k)} \tag{6}$$

In addition, as an advanced wireless communication method, full-duplex system may face the same issues as the traditional half-duplex counterpart. The issues include the phase rotation in the received signal cased by the sample frequency offset and center frequency offset, signal fading and inter-symbol interference caused by the complex wireless channel. Traditional corresponding solutions also apply to the full-duplex wireless communication, so they won't be covered in this paper.

2.2 802.11 PHY & MAC introduction

The PHY layer of 802.11 protocol is mainly based on the orthogonal frequency division multiplexing (OFDM) technology. OFDM has high spectral efficiency compared to other modulation schemes, and can effectively adapt to complex channel conditions with simple frequency-domain equalization [2].

The subcarriers in 802.11a are BPSK, QPSK, 16-QAM, 64-QAM modulated, and the coding rates include 1/2, 2/3, 3/4. A certain kind of modulation type and coding rate determines one of the eight supported data rates, as showed in Table 1. Each OFDM symbol consists of 48 complex data values, 4 pilot signals, and 12 unused carriers. This group of subcarriers is transformed into the time domain symbol by 64 point IFFT, and a 16 point cyclic prefix is prepended to the symbol. Thus, each 802.11a symbol consists of 80 complex time-domain data samples. As the sampling rate in 802.11a is 20MHz, the duration of one symbol in 802.11a is 4us in total [2].

The 802.11a frame structure consists of short training field (STF), long training field (LTF), and signal field (SIG), followed by the Service, DATA and Tail field. 32bit cyclic redundancy check (CRC) is attached at the end of the DATA field. For standard WiFi, STF is used for automatic gain control (AGC) and coarse timing & frequency timing synchronizations. LTF is used for channel estimation and accurate timing synchronizations. SIG contains the coding rate and length information for a frame. Useful information is placed in the DATA field, and CRC checksum is used to validate the integrity of a frame. Since the contents of Service and Tail field are always zero, in the following sections, we roughly use DATA field to indicate fields of Service, DATA and Tail [2].

Table 1 Supported rates in 802.11a

Modulation type	Coding rate	802.11a data rate (Mbps)
BPSK	1/2	6
BPSK	3/4	9
QPSK	1/2	12
QPSK	3/4	18
16-QAM	1/2	24
16-QAM	3/4	36
64-QAM	2/3	48
64-QAM	3/4	54

Figure 2 illustrates the 802.11a frame structure.

The 802.11 medium access control (MAC) supports shared wireless medium access through the celebrated mechanism of carrier sense multiple access with collision avoidance (CSMA/CA) [2]. Once the medium changes to idle, WiFi device needs to defer a random period (called backoff time), continues to detect the channel state, and it begins to transmit signals if the medium is still idle at the end of the backoff time. Other devices failed to access the medium would likely to choose another time to start transmission. This mechanism significantly reduces the rates of frame collision.

For full-duplex WiFi, to coexist with the commercial WiFi devices, one should follow the basic 802.11a/g MAC & PHY protocol.

2.3 Related work

Several full-duplex platforms have been proposed. They include GNU Radio [1], WARP [5, 7, 8], and WARPLAB [6]. In this subsection, these three existing platforms will be discussed in detail.

Specifically, GNU Radio is a pure software-based platform. Users can design their own arithmetic modules by writing C++ code. With an external USRP RF front-end, Researchers can quickly implement a novel wireless transceiver. However, GNU Radio is not suitable to develop full-duplex WiFi for the following reasons. (1) It only supports real-time throughput up to a few Mbps, and the frame interaction interval can reach up to several us, far below the requirement of current WiFi standards [3] (e.g. 802.11a/g requires 54Mbps data rate, and less than 16us acknowledge time). (2) GNU Radio can easily organize modules

Fig. 2 802.11a frame structure

into pipeline structure, but performs badly in realizing the feedback architecture and handling the communications between two remote modules. The latter two cases are frequently encountered in full-duplex WiFi design.

Second, WARP is a popular, hardware-based full-duplex platform [5, 7, 8]. WARP leverages FPGA to accelerate wireless algorithms with massive computations, which provides higher performance than GNU Radio. It can work in 20MHz bandwidth, but the frame response latency is large (75us) [5]. It thus fails to meet the SIFS timing requirement. Moreover, WARP does not provide support for modular design, which results in the lack of flexibility.

Third, WARPLAB is a software-based platform, which uses MATLAB to implement the full-duplex algorithm. Its performance is not appealing, since its processing delay can reach up to 50ms [6], three orders of magnitude higher than the WiFi requirement.

Table 2 provides an overview of different platforms.

In summary, none of the recent platforms, no matter whether it is based on software or relies on hardware, is suitable for full-duplex WiFi.

3 Design

From the previous point of view, researchers who study full-duplex WiFi desire a platform that provides flexibility and real-time features. However, it is difficult to meet the two goals simultaneously, and we will face several challenges. In this section, we will provide a detailed description of the design of GRT-duplex platform, and show how to tackle these challenges. Moreover, we will describe the frame interaction design applied in full-duplex WiFi.

Table 2 Comparison of different platforms

Platforms	Flexibility	Real-time
GNU Radio	-software based. -designed by C++. -limited to the pipeline structure.	-throughput up to a few Mbps.
WARP	-hardware based. -do not provide special support to modular design.	-bandwidth:20MHz. -latency:75us.
WARPLAB	-software based. -designed by MATLAB.	-processing delay: 50ms
Custom chips	-no exibility.	-work in real-time.
GRT-duplex	-hardware based. -support modular design.	-work in real-time. -bandwidth:20MHz. -latency:9.85us.

3.1 Design challenges

To meet both goals of flexibility and real-time processing, we have identified three challenges.

First, it is difficult for a platform to achieve both goals simultaneously. In the platforms based on software, CPU processing is the main bottleneck. Although software platforms have good programmability, they cannot ensure real-time operation of the state-of-the-art wireless protocols, both in throughput and latency. On the other hand, platforms based on hardware have high performance, but with their fixed logic structure, it is hard to change any instance of full-duplex WiFi implementation. In both cases, a novel platform architecture for full-duplex WiFi is desired.

Second, full-duplex WiFi platform should provide flexible APIs. In general, a full-duplex WiFi system consists of several components, including PHY, MAC, radio-frequency (RF) front-end and host computer for control purposes. In different usage settings, researchers may demand different connections among modules. Flexible interfaces between components are a must.

Third, in order to enable digital cancellation, we need to estimate both target and interference channels. More redundant training parts imply better channel estimation results, but lower frame transmission efficiency. How to design effective frame interaction thus becomes critical.

3.2 Design of GRT-duplex platform

Modular design is applied at the PHY layer of the GRT-duplex platform to address the first challenge. Each PHY module works as an independent arithmetic unit. Using general asynchronous FIFO, signals can transmit between every pair of modules, and each module can operate in its own clock domain.

This modular structure design ensures the independence of each module. First, to optimize the performance of the whole system, users only need to achieve optimal performance of each module without considering the details of interaction between them. In this way, the system can easily meet the requirement of real-time processing capability. Second, this design provides great flexibility to users. With asynchronous FIFO, the SDR system can provide the method of inserting, modifying and removing one or more modules. Noted that the interface of each module may be configured as multiple inputs/outputs, users can connect these modules at will, and easily implement the complex mesh connection structure.

For full-duplex WiFi, the receiver needs to obtain the signals from its own transmitter. Connection from a module in transmitter to a module in receiver is needed. Considering another scenario, MIMO owned the structure of merge and divert. Without the flexible structure, researchers are

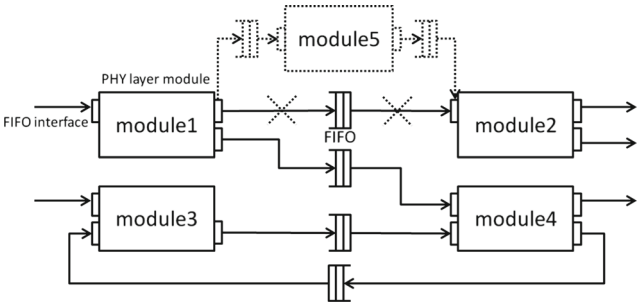

Fig. 3 A special architecture of PHY layer module connection

restricted to achieve some simple PHY layer structure like pipeline.

Figure 3 illustrates the architecture of PHY layer module connection. Each module has one or more inputs/outputs. For example, if one wants to insert module5 between module1 and module2, all he needs to do is to disconnect the prior connection FIFO, and to directly insert module5. This flexible modular design can substantiate most of the PHY design, not only full-duplex wireless, but also MIMO and other heterogeneous PHY architectures [4, 13, 14].

We use different interfaces to ensure flexible connections. GRT-duplex consists of four parts, PHY layer and MAC layer, RF front-end and host computer, showed in Fig. 4. Three types of interactive interfaces are supported between each part, including DMA, PIO and Interrupt, to meet the diverse requirements.

Specifically, DMA interface supports high-speed data streams. All data streams are transmitted by DMA, including the data exchanges between Host PC and FPGA, and the signal samples transfer between FPGA and RF front-end. In addition, we can use the DMA interface to attain the intermediate result generated from any module in real-time. For example, we can acquire of constellation mapping or frequency-domain information at any time.

PIO interface can transfer some state information, for example, coding rate and frame length from host computer to FPGA, CRC check result and bit error rate statistics from FPGA to host computer.

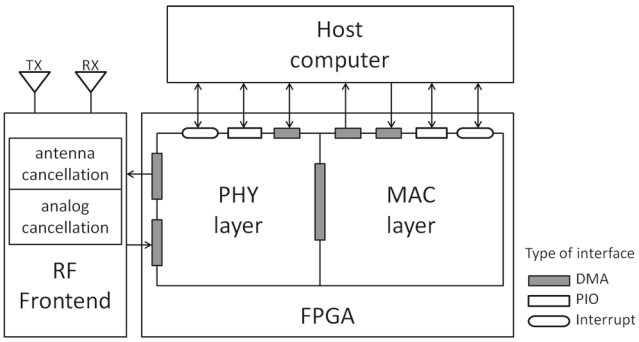

Fig. 4 Architecture of GRT-duplex

Interrupt interface ensures low-latency control, once a FPGA obtains a frame, it may request an interrupt to the computer, and the host computer should react to the frame as soon as possible.

Some APIs provided to users are listed as follows.

```
int dma_host2board(unsigned int len, void
*p_data);
int dma_board2host(unsigned int len, void
*p_data);
int read_usr_reg(unsigned int reg, unsigned
int *p_data);
int write_usr_reg(unsigned int reg, unsigned
int *p_data);
int block_until_interrupt(int vector_num);
```

The front-end part can connect to GRT-duplex via the DMA interface. It contains analog cancellation and antenna cancellation module. With the two-step cancellation, certain amount of self-interference can be eliminated. Using this flexible interface, different RF front-end can apply to the same PHY layer design.

In summary, we have proposed a novel modular structure based on hardware to ensure real-time performance and flexibility. This design makes it suitable for full-duplex WiFi research.

3.3 Design of frame interaction

The design of effective frame interaction is critical to full-duplex WiFi. In order to enable digital cancellation, we need to estimate both target and interference channels. When two devices work in the full-duplex mode, the target signal and the interference signal are mixed together, thus unable to invoke channel estimation. Therefore, we have to design a new frame interaction. Figure 5 depicts the detailed frame structure.

Full-duplex MAC uses the point coordination interactive mechanism. Different from the half-duplex WiFi, AP works as an active equipment, centralized manages the whole devices associated with it; Whereas, Devices are absolutely scheduled by an AP. To start full-duplex data exchanges, AP and a Device must transmit a training frame separately. First, AP issues a request frame, while the AP and the Device estimate interference channel and target channel separately. Then, the Device issues a response frame, while the AP and the Device estimate target channel and interference channel separately. After the two-way handshake, AP and Device transmit and receive an equal length frame simultaneously. 32-bit CRC is used to validate the correctness of the received frame. Retransmissions are invoked upon a CRC error.

Both the training parts and the full-duplex data parts are standard 802.11a frames. Thus, other non-full-duplex

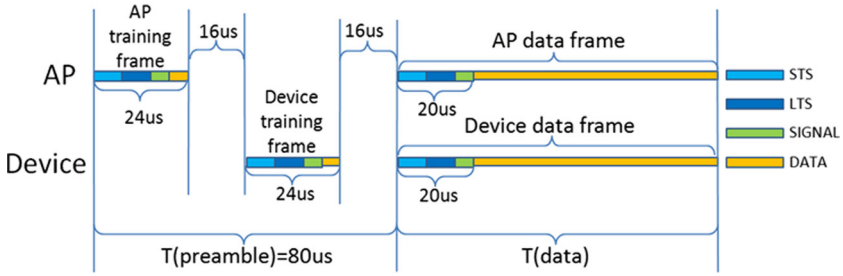

Fig. 5 Design of frame interaction

devices can demodulate the full-duplex frame, and a full-duplex device can act as a non-full-duplex device before the two-way handshake. Before the full-duplex device transmits a training frame, it should first finish the backoff procedure. SIFS time (16us) has been used to ensure that the full-duplex devices can work in a non-full-duplex WiFi environment.

Figure 6 is a timing chart shows the basic process of a frame exchange in full-duplex WiFi. If an AP detects the medium goes to idle, AP delays a time of DIFS + random backoff. If the medium continues to idle in this period, AP and Device start to exchange a frame, otherwise continues to delay. A Device must actively synchronize to the AP, and transmit the data frame simultaneously. We can see once a full-duplex AP gained access to the medium, it maintains control of the medium by keeping a SIFS, thus can coexist with the state-of-art WiFi equipments.

4 Implementation

4.1 Implementation challenges

To enable full-duplex WiFi, we need to tackle two challenges.

First, none of the existing WiFi implementations can easily extend to realize full-duplex WiFi, because of the lack of flexibility. Think over the legacy WiFi, the transmitter and receiver part is completely independent, there are no data interactions between them. Moreover, both transmitter and receiver have a simple pipeline structure. Finishing all the arithmetic modules of WiFi and combine them together, one can achieve a WiFi system. However, full-duplex WiFi contains the new modules of self-interference cancellation, also needs to transfer data streams from transmitter to receiver. General hardware-based platform without flexibility seems hard to insert or modify a module, let alone to build a complex PHY architecture.

Second, the modular structure should be carefully implemented to meet the real-time processing requirement. Performance of both throughput and latency should be carefully considered. As mentioned in previous sections, data throughput needs to exceed 54Mbps, and data response time should be smaller than 16us. Thus performance of each module should over the throughput of minimum requirement, and the total latency of the whole modules needs to be low.

There are a lot of implementations for WiFi exist. Commercial WiFi network cards use existing chips to realize processing algorithms of WiFi. Researchers never know the internal details of WiFi chips, and can't program on them. WiFi implementations based on other platforms failed to meet the real-time and flexible requirements simultaneously. Since existing WiFi implementations cannot be used, we have implemented the full 802.11a module library before starting the full-duplex WiFi implementation.

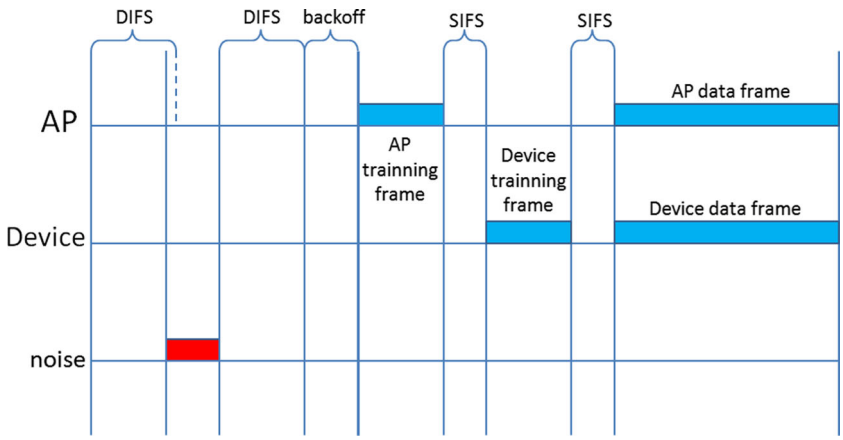

Fig. 6 MAC design for full-duplex WiFi

Table 3 Modules in GRT-duplex library

Name of modules	Tx/Rx
Scrambler	Tx
BCC (Block Convolutional Code)	Tx
Puncture	Tx
Interleaver	Tx
Constellation	Tx
Insert_Pilot	Tx
IFFT	Tx
Insert_GI (Insert Guard Interval)	Tx
Timing_Synchronization	Rx
Frequency_Synchronization	Rx
Remove_GI	Rx
FFT	Rx
Channel_Estimation	Rx
Phase_Tracking	Rx
Deconstellation	Rx
Deinterleaver	Rx
Depuncture	Rx
Viterbi_Decoder	Rx
Descrambler	Rx

4.2 Real-time assurance

To meet the real-time processing challenge, we have considered two factors.

First, we have implemented a flexible hardware architecture, since each module can operate at its highest clock frequency, we can maximize the throughput and minimize the latency.

Second, when selecting the RF front-end, we have looked into both USRP N210 and FMC AD9361. USRP N210 uses the Ethernet cable to transfer data and control information simultaneously, thus incurring high latency [12]. Experimental result showed that, the Ethernet cable caused at least 20∼30us delay, and cannot meet the SIFS timing requirements (16us) in the full-duplex WiFi. We consequently have chosen the FMC AD9361 RF front-end with less than 2us delay.

4.3 Implementation of GRT-duplex library

Before realizing full-duplex WiFi, we first complete the GRT-duplex library, which contains one module for MAC layer (32-bit CRC check) and 19 modules for PHY layer. Researchers can implement standard WiFi protocol using the modules in the library. Table 3 shows the PHY modules for WiFi.

Using these modules based on GRT-duplex platform, with 802.11 driver running in host computer, the system can work in standard WiFi mode. Former experiments showed the system can work in real-time and can connect to commercial WiFi devices [10]. This indicates that GRT-duplex can work in high performance, at least the same magnitude with state-of-art wireless protocol.

4.4 Implementation of full-duplex WiFi

Using the GRT-duplex library, we added and modified some modules, and implemented the full-duplex WiFi. PHY layer and MAC layer based on GRT-duplex have been implemented on the Xilinx ZC706 Evaluation board. We instrumented two FMC AD9361 front-ends with antenna and analog cancellation setups. We also used a PC to detect the full-duplex working state and control the operation mode via PIO interface. We wrote the Verilog HDL code in VIVADO 2013.4. We used the existing equipment to implement both analog cancellation and antenna cancellation. These two parts can remove 40∼50dB of self-interference through the cancellation algorithm.

Figure 7 plots the main hardware architecture of full-duplex WiFi based on GRT-duplex. The black modules represent the GRT-duplex modules provided in the library, and the green parts denote the new modules or modified modules implemented for full-duplex. We can see that, one only needs to do a few modifications to implement full-duplex WiFi.

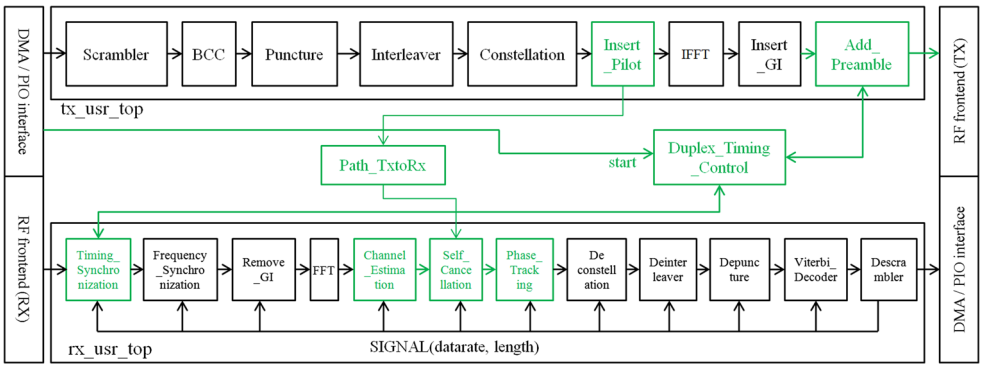

Fig. 7 Implementation of full-duplex WiFi based on GRT-duplex

Specifically, the module Add_Preamble generates AP and Device training frames. In module Channel_Estimation, both the target and the interference channel have been estimated, and in Self_Cancellation module, the calculation in Eq. 6 has been implemented. We use module Path_TxtoRx to transfer its own transmitted signals in the frequency domain (signals before IFFT) to Self_Cancellation module. The modules of Duplex_Timing_Control, Add_Preamble and Timing_Synchronization collaborate to ensure the proper timing for frame interactions, depicted in Figs. 5 and 6.

In general, we have not only provided a full WiFi module library, but also implemented a novel PHY architecture. So it is easy for researchers to develop and validate their new ideas of full-duplex WiFi on GRT-duplex.

5 Evaluation

5.1 Experimental setup

Using the GRT-duplex platform, users are free to set the center frequency, sample rate, and TX & RX gains from PIO interface. We further support all data rates (6∼54Mbps) and lengths (1∼4095byte) in the 802.11a protocol. Each GRT-duplex can work as an AP or a Device through PIO configuration. In our experiment, we used all 8 modulation schemes in 802.11a, and 1500B data length to assess our full-duplex WiFi system. We selected 2.457GHz as the center frequency and 20MHz being the sampling rate. These configuration parameters are identical to commercial WiFi devices working on Channel 10. The CRC results at the MAC layer indicate whether a frame has been successfully received. Figure 8 shows a picture of the full-duplex WiFi system based on GRT-duplex.

We implemented the GRT-duplex WiFi with XC7Z045 FPGA in Xilinx ZC706 evaluation board. Table 4 shows the resource consumption.

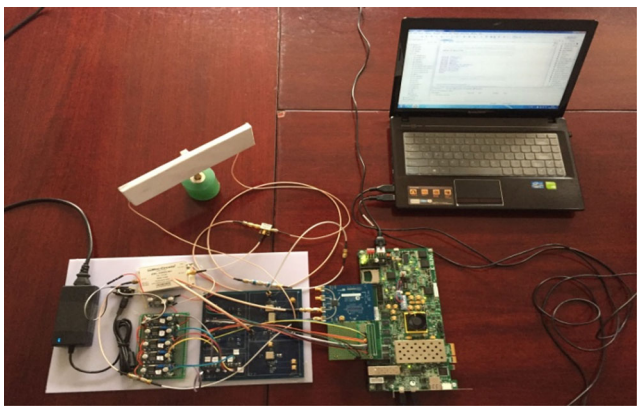

Fig. 8 Full-duplex WiFi system based on GRT-duplex

Table 4 Full-duplex WiFi resource consumption

Resource	Used	Available
slice LUTs	70454(32 %)	218600
slice registers	41048(9 %)	437200

5.2 Flexibility evaluation

GRT-duplex has provided 19 modules for the standard 802.11a protocol [9–11]. To achieve full-duplex WiFi, we modified four modules in the module library (Timing_Synchronization, Channel_Estimation, Phase_Tracking and Insert_Pilot), and added four extra modules for digital cancellation (Self_Cancellation, Path_TxtoRx, Duplex_Timing_Control and Add_Preamble).

The following pie chart in Fig. 9 depicts the distribution of codes for full-duplex WiFi. There is 6 % new added code and 2 % modified code.

Through the above analysis, we find that 92 % of the code for current WiFi can be reused.

5.3 Constellation mapping

As mentioned before, with the flexible structure, we can acquire any intermediate result in real-time using GRT-duplex platform. To observe the result of digital cancellation visually, we collected three sets of the constellation mapping signals in real-time, then we plot them offline using MATLAB. In this process, we set the modulation scheme of transmit signals to 16-QAM, the signal bandwidth was 20MHz, and the center frequency has been set to 2.457GHz.

Figure 10 represents the received superimposed signal in frequency-domain. Affected by residual interference signal, receiver's noise, channel fading and frequency offset, random scatter of the signal shows in the constellation map. It is obvious that without eliminating the interference signal, the target signal can't be distinguished.

Figure 11 shows the signal after the self-interference cancellation. After this operation, we can roughly see the

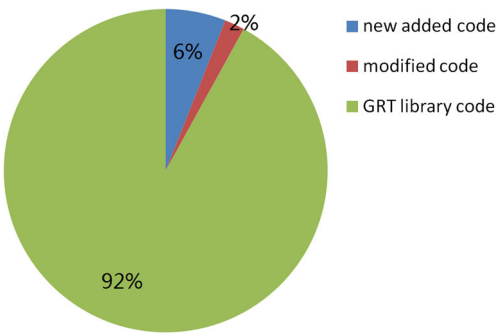

Fig. 9 Statistical chart of full-duplex WiFi

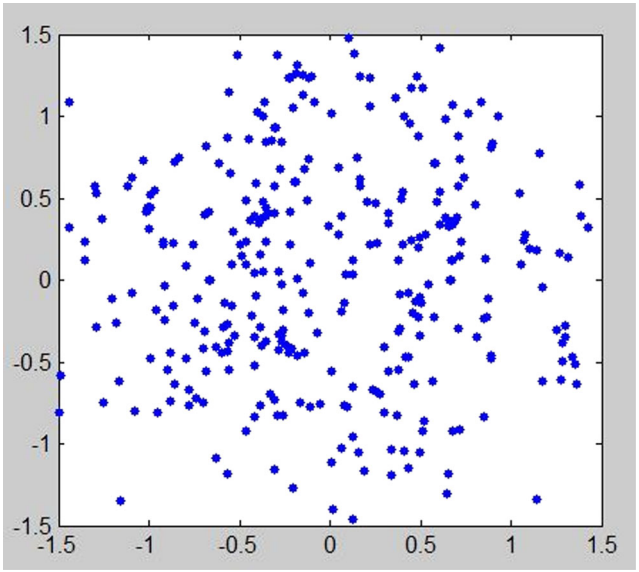

Fig. 10 Constellation mapping before digital cancellation

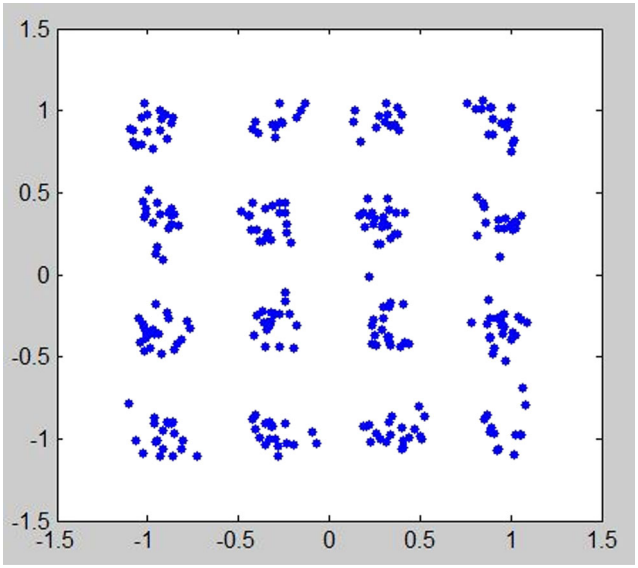

Fig. 12 Constellation mapping after phase tracking

signal's amplitude showing the 16-QAM features. But due to the residual frequency offset, the phase of the signal has been rotated.

Based on the signal in Fig. 11, we make further phase compensation with 4 pilots in subcarrier, and the result shows in Fig. 12. After phase correction process, we can see a clear pattern of 16-QAM. So the receiver can properly complete the constellation demapping process.

Moreover, transmitting and receiving clock is the same for the interference signal, so there is no frequency offset problems exist.

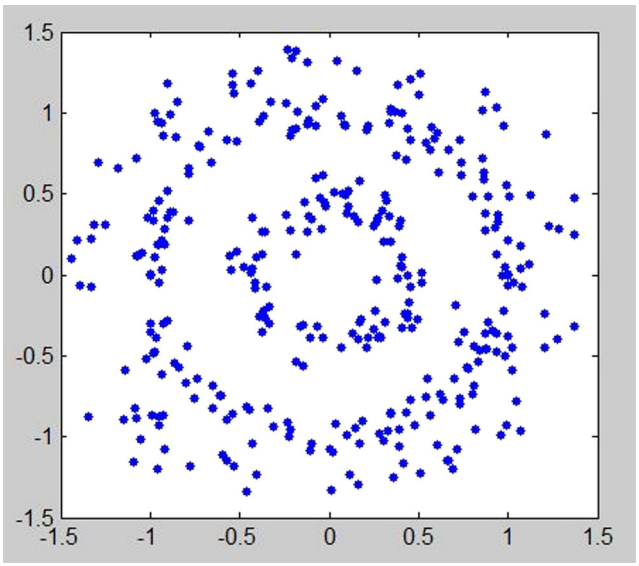

Fig. 11 Constellation mapping after digital cancellation

Using GRT-duplex, we can obtain any intermediate signal in real-time, the flexibility of this platform is also reflected here.

5.4 Real-time transmition evaluation

In our experiment, a Device can respond to a request within 9.85us. To reply a frame by the deadline of 16us, we added an extra delay of 6.15us. This shows that, the processing delay of GRT-duplex can meet the requirement of the standard 802.11a WiFi.

Regarding the training frame overhead, we tested the theoretical throughput at the MAC layer and presented the results in Table 5. We achieve 1.71∼1.96x throughput improvements compared with the half-duplex WiFi system.

When more sophisticated modulation is used, the effective transmission time for the data part becomes shorter. The redundancy of the training part will have more impact on performance. We used 8 modulations. The obtained CRC results indicated that our full-duplex WiFi system successfully received the correct signal in different sending modes.

6 Discussion

In this paper, we do not focus on full-duplex itself, including full duplex baseband algorithms, antenna and analog cancellation. Therefore, we used existing full-duplex RF device and implemented a relatively simple digital cancellation algorithm. Although we have demodulated 64-QAM signals in full-duplex mode, there is still some room for algorithm optimization. We provide GRT-duplex mainly for

Table 5 Theoretical throughput test

Modulation type	Coding rate	802.11a throughput (Mbps)	Full-duplex WiFi throughput (Mbps)	Performance improvement
BPSK	1/2	6	11.76	1.96
BPSK	3/4	9	17.48	1.94
QPSK	1/2	12	23.11	1.93
QPSK	3/4	18	34.02	1.89
16-QAM	1/2	24	44.59	1.86
16-QAM	3/4	36	64.68	1.80
64-QAM	2/3	48	83.49	1.74
64-QAM	3/4	54	92.45	1.71

researchers who study full-duplex WiFi. They can make use of this platform for further research.

Two features of GRT-duplex have mainly been discussed in this paper.

Flexibility For full-duplex researchers, flexibility is a very important feature. Firstly, we adopted modular design concept, researchers can easily add, delete, or modify any module, and connect these modules at will. Thus it allows users to have great degree of freedom to complete their new algorithm design without concerning about detailed issues in hardware design. According to the assessment result, based on the GRT-duplex library, only 8 % of the code has been changed. This greatly reduces the development time. So, users can pay more effort within full-duplex design, thus significantly enhance the development efficiency.

Secondly, the interface design ensures flexible connections. Different full-duplex implementation may adopt different full-duplex RF front-end. GRT-duplex allows users to select diverse equipment of antenna and analog cancellation. According to our experiments, Both USRP and FMC AD9361 can apply to the GRT-duplex system. On the other hand, flexible connections provide convenient ways for users to interact with GRT-duplex. Different interfaces can meet the diverse requirements. Specifically, through PIO configuration, we can set the different working mode. With DMA transmission, we can acquire any data streams generated from modules. This feature provides great convenience to researchers for testing the system's performance or debugging system.

Real-time Real-time is also an important factor of a full-duplex WiFi platform. In order to verify a new full-duplex algorithm, researcher may first choose to simulate based on software, for example, MATLAB. However, the real wireless environment is much more complicated than the simulation model, without testing in real-time, researchers may fail to take into account some special channel conditions. Recently, there are some real-time system operating in low bandwidth. Even if transmission is correct in low bandwidth, when bandwidth becomes wide, the requirement for baseband design will become higher because of the frequency selective fading channel and the higher frequency offset. Therefore, only with the use of real-time platform, we can attain the most accurate test results.

In fact, performance of throughput and latency depends on each module design by users. Since we adopt the modular design concept, there is no dependency between these modules. To achieve highest performance, users only need to optimize their own modules to the desired performance. Evaluation of GRT-duplex delivers throughput up to 92.45Mbps, and the latency can be as small as 9.85us, fully supports real-time requirements of full-duplex WiFi.

Complexity and cost The complexity and development costs to achieve full-duplex WiFi have been greatly reduced due to its flexibility. In contrast, WARP does not support modular design, and users have to handle and configure the interfaces between different modules. According to our assessment result, one only needs to modify 8 % of the code to achieve full-duplex in our implementation. Moreover, WARP does not provide flexible interfaces for users and the RF front-end. It is thus difficult for WARP to work with other peripherals.

The cost of our GRT-duplex platform mainly includes the parts of antenna, analog circuit, FMC RF front-end, FPGA evaluation board and host computer. The used antenna, analog circuit and RF front-end are all lightweight peripherals. In contrast, although the complexity and the cost are relatively low in software-based platforms, non-real-time is still the main bottleneck.

Our contribution is to provide a real-time, flexible full-duplex WiFi platform. Full-duplex researchers can use the system to complete their unique design. In addition, we designed a full-duplex frame interaction mechanism, so GRT-duplex is compatible with traditional WiFi. Finally, we provide a standard GRT-duplex library. The library supports standard WiFi protocol, and can be easily extended to full-duplex implementation.

With the rapid development of wireless protocols, the full-duplex WiFi platforms with higher rates will be needed soon. So we may further optimize our GRT-duplex platform to support new generated WiFi protocols and MIMO systems.

7 Conclusion

In this paper, we have proposed GRT-duplex, a flexible and real-time full-duplex wireless platform. Unlike prior designs, GRT-duplex platform provides both *flexibility* and *real-time* features. It is well suited for full-duplex WiFi research. GRT-duplex provides complete library for 802.11a and uses flexible hardware architecture. It also works in real time. Our current prototype of full-duplex WiFi delivers throughput up to 92.45Mbps, and the frame interaction intervals can be as small as 9.85us.

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